RAMAIAH
College of Arts, Science
& Commerce - Autonomous

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ANALOG AND DIGITAL ELECTRONICS-I -LAB MANUAL
Course Code:24ELEP102
I SEMESTER B.Sc.(EMC) PAPER I

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DEPARTMENT OF ELECTRONICS

LAB RULES

- **Students are not allowed to carry bags inside the lab.**
- **Loitering and throwing litter in the lab is strictly prohibited.**
- **Usage of mobile phones within the lab is restricted.**
- **The required lab equipment and components are to be used only with lab assistant supervision.**
- **The students should maintain the lab manuals and up-to-date instructions given by the lab in-charge.**
- **Use the lab equipment only after instructions given by the lab in-charge.**
- **While leaving the lab, return the electronic components used in the experiments and arrange the chairs.**
- **A student must take care of lab equipment and is expected to protect it from getting damaged/vandalized.**
- **Do not change the settings of equipment without lab in-charge permission.**
- **Students should maintain lab observation during the lab hours.**
- **Fans and lights should be switched off after use.**

EXPERIMENT NO – 1

Verification of Superposition Theorem

Aim: To experimentally verify superposition theorem.

Components and Equipment: DC power supply (0-15) V, (0-25)mA Milli Ammeter, resistors-220 Ω (2), 330 Ω, multimeter, breadboard.

Statement: Superposition theorem states that the current through or the voltage across an element in a linear, bilateral network consisting of several sources is equal to the algebraic sum of the currents or voltages respectively produced independently by each source.

Procedure: Circuit connections are made as shown in the Fig (i). Both the supplies are switched on and adjusted to the given values. The current reading, I in the millimeter is noted. To consider the effect of each source acting independently, V_B is shorted as shown in Fig (ii) and with only V_A acting, the current I_1 is noted. The current I_2 through the same branch is noted by shorting the supply V_A as shown in Fig(iii) and only V_B acting. It is observed that $I = I_1 + I_2$ thus verifying superposition theorem. The voltages V, V_1 and V_2 are also noted. It is observed that $V = V_1 + V_2$. The experiment is repeated with different values of V_A and V_B.

Result: Superposition Theorem is experimentally verified.

CIRCUIT DIAGRAM

To Find I and V

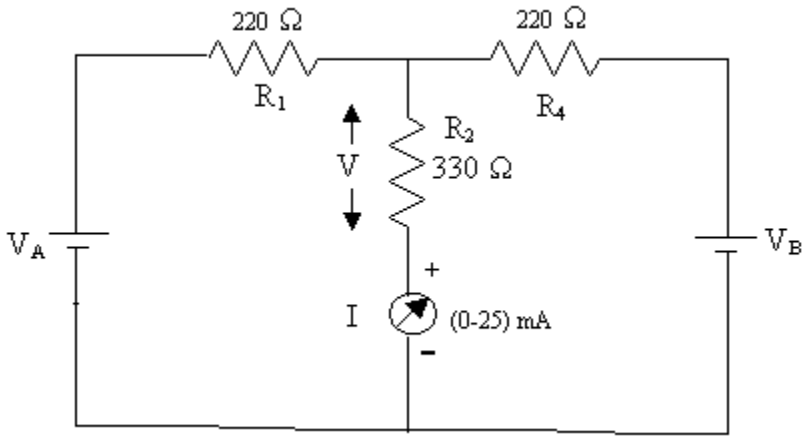
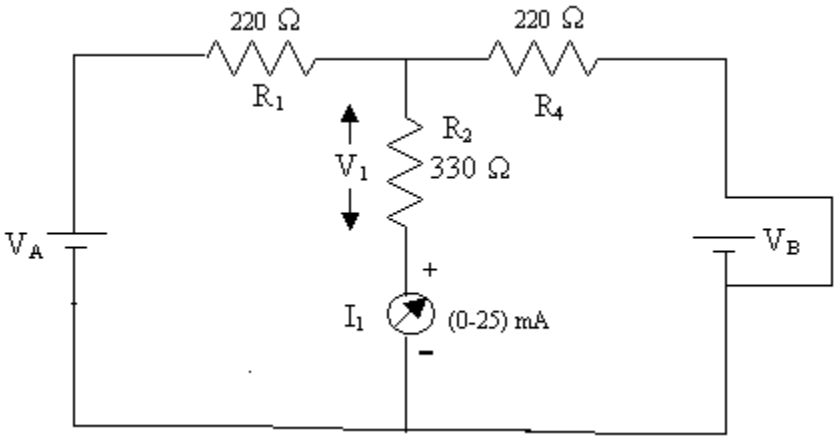


Fig (i)

To Find I_1 and V_1



Fig(ii)

To Find I_2 and V_2

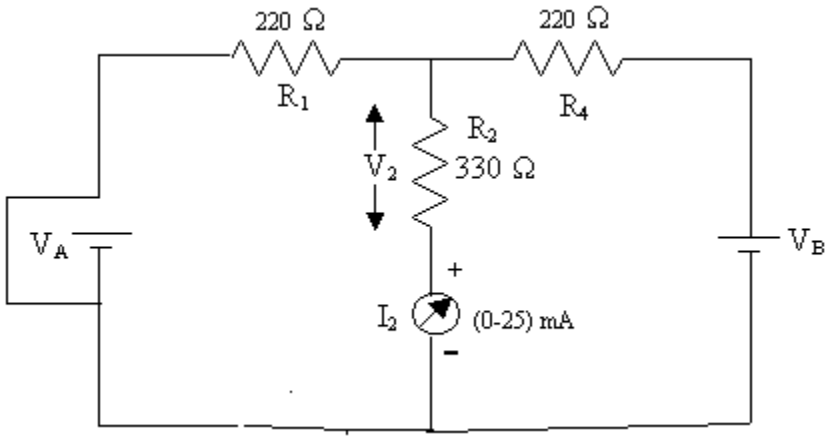


Fig (iii)

Tabular Column

Trial No.	V_A (V)	V_B (V)	I (mA)	I_1 (mA)	I_2 (mA)	$I= I_1+ I_2$ (mA)	V (V)	V_1 (V)	V_2 (V)	$V=V_1+V_2$ (V)
1										
2										
3										

EXPERIMENT NO - 2

Verification of Thevenin's and Maximum Transfer Theorem

Aim: To verify Thevenin's and Maximum Transfer theorem.

Equipment's and components: Regulated Power Supply (0 – 10 volts), ½ watt resistors 330Ω, 100Ω, 220Ω, digital millimeter (0-10mA) range, Decade resistor box, bread board, connecting wires, digital multimeter.

Principle:

The Thevenin voltage (V_{Th}) is defined as the voltage measured across the load terminals of the given circuit when the load resistor is open.

The Thevenin Resistance (R_{Th}) is defined as the resistance an ohmmeter measures across the load terminals of the given circuit when all the voltage sources are reduced to zero voltage and the load resistor is open.

Thevenin's theorem- A two terminal linear network can be replaced by an equivalent circuit consisting of a single voltage source (V_{Th}) and a series resistor (R_{Th}).

Maximum Power transfer Theorem: In any linear two terminal bilateral networks the power delivered to the load from source is maximum when load resistance is equal to the internal resistance of the network or thevenin's resistance of the circuit.

Formula:

Instead of measuring the Thevenin voltage (V_{Th}), it can be calculated also

From the circuit (1) $V_{Th} = \frac{(VR_2)}{(R_1+R_2)}$

Instead of measuring the Thevenin resistance (R_{Th}), it can be calculated also

From the circuit (1) $R_{Th} = \frac{R_1R_2}{(R_1+R_2)} + R_3$

For the maximum power transfer to occur $R_L = R_{Th}$

Then maximum power delivered to the load resistance is given by, $P_{max} = \frac{V_{Th}^2}{4R_{Th}}$

Procedure:

(a) <u>For the given circuit</u>

1. Adjust the voltage (E) of the regulated power supply to 1 volt and Construct the circuit (1).
2. Measure the load current (I_L) with the digital milliammeter, tabulate it.
3. Similarly tabulate I_L for different E values, namely E = 2V, 3V and 4V one after the other. I_L is load current of the original circuit given.

(b) <u>For the Thevenin equivalent circuit</u>

1. Measure R_1, R_2 and R_3 with a multimeter.
2. By using the formula, calculate V_{Th} when E =1V, E =2V, E = 3V and E = 4V. Also calculate R_{Th}.
3. Arrange R_{Th} in the decade resistor box. Construct the circuit (2).
4. Adjust the voltage of the power supply as the first calculated value of V_{Th} and measure load current (I_L') from the milliammeter. Tabulate it in the first row.
5. Similarly note I_L' for the other calculated V_{Th} values and tabulate them in the respective rows. I_L' is the load current of the Thevenin equivalent circuit.
6. Compare I_L and I_L' to verify thevenin's theorem. If $I_L = I_L$', the theorem is verified.

(c) For Maximum Power Transfer Theorem

1. Circuit is constructed as shown in the figure.

2. Set the input voltage (RPS) to 5V.

3. Vary the value of load resistance (RL) in steps of 100Ω

4. Measure the current [IL] through and voltage [VL] across the load using milliammeter and DMM respectively and tabulate the values.

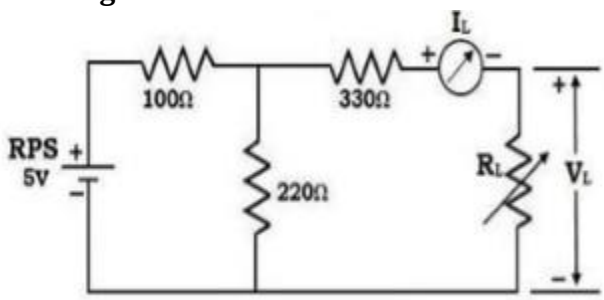
5. Calculate the power using the formula PL=VL x IL

6. To find Rth: replace RPS by short circuit, remove the load RL and measure the total resistance of the circuit (Rth) across the open circuit using DMM.

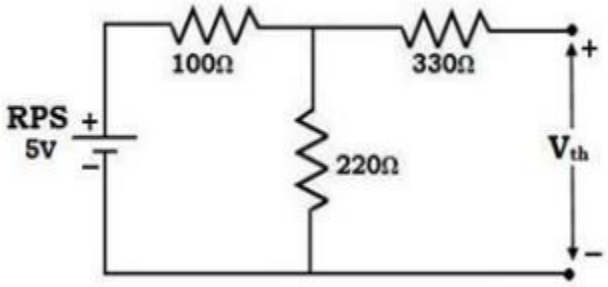
7. A graph is drawn showing the power PL against load [RL]

Result : The Thevenin's theorem and Maximum Transfer Theorem verified.

Circuit Diagram:



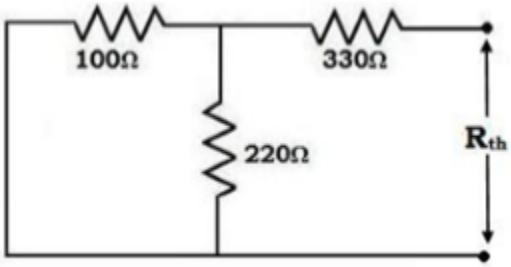
To find V_{th}:



Vth(Theoretical)=_____(volt)

Vth(Practical)=_____(volt)

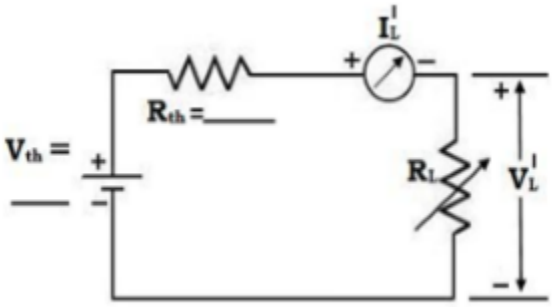
To find Rth:



Rth (Theoretical)=_____ (Ω)

Rth(Practical)=_____(Ω)

Thevinin's equivalent circuit:



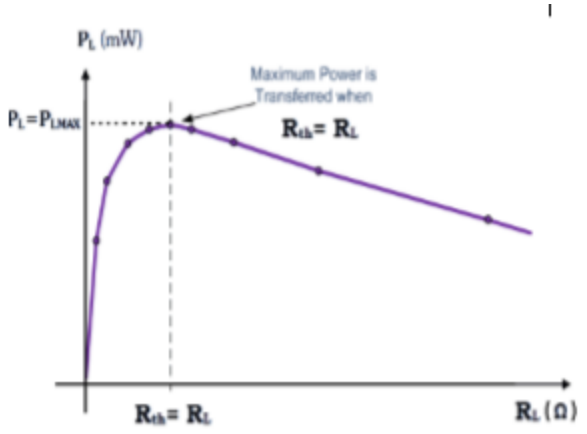
Tabular Column-: For Thevenin's Theorem

R_L (Ω)	V_L (V)	I_L (mA)	V_L' (V)	I_L' (mA)
100				
200				
300				
400				
500				
600				
700				
800				
900				
1000				

For Maximum Power Transfer Theorem

R_L (Ω)	V_L (V)	I_L (mA)	$P_L = V_L \times I_L$ (mW)
100			
200			
300			
400			
500			
600			
700			
800			
900			
1000			

Model Graph-:



EXPERIMENT NO – 3

Study of IV Characteristics of a) pn junction diode b) zener diode

a) pn junction diode

Aim: To study the I-V Characteristics of p-n junction Diode

Components and Equipment: Diode, Resistor (470Ω), Power Supply, DMM, milliammeter Bread Board and connecting wires.

Theory: A semiconductor diode is a p-n junction device which will conduct only when it is forward biased where as it will offer high resistance for the flow of the current when it is reverse biased.

Procedure:

Forward Biased Condition:

1. Connect the circuit as shown in figure (1) using silicon PN Junction diode.

2. Vary Vf gradually in steps of 0.1 volts upto 5 volts and note down the corresponding readings of If .

3. Step Size is not fixed because of nonlinear curve and vary the X-axis variable (i.e. if output variation is more, decrease input step size and vice versa).

4. Tabulate different forward currents obtained for different forward voltages

Result:

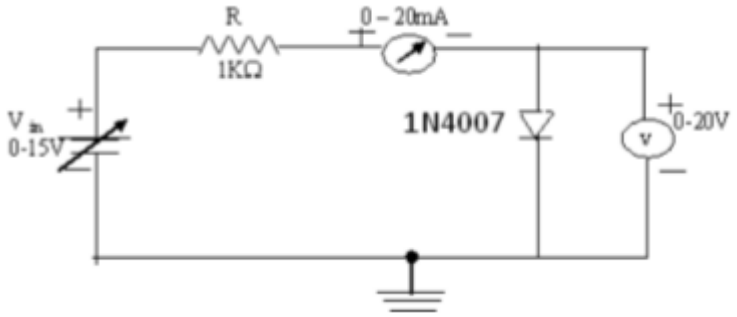
V -I characteristics of a p-n junction diode is drawn and it is found that,

1. Dynamic resistance, RD = _____ Ω

2. Static resistance, RS = _____ Ω

3. Knee voltage, VK = _____ V

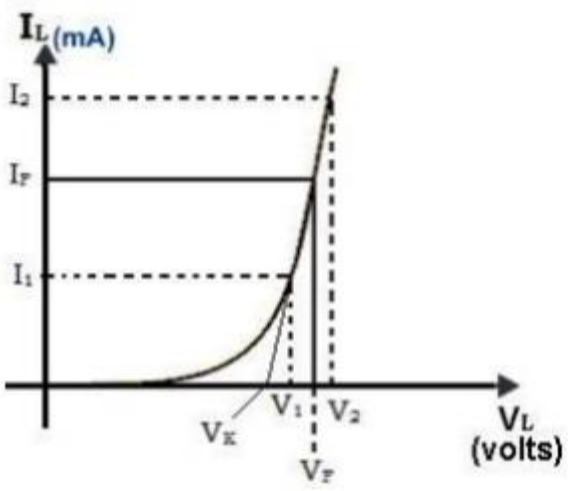
Circuit Diagram for Forward bias:



Tabular Column-:

Vi	Vf	If

Model Graph-:



From graph:

1. Knee Voltage V_K=----------V
2.
3. Dynamic resistance, R_D

$$R_D = \frac{V_2 - V_1}{I_2 - I_1} = \_\_\_\_\_ \Omega$$

4. Static resistance, R_S=

$$R_S = \frac{V_F}{I_F} = \_\_\_\_\_ \Omega$$

b) Zener diode-:

Aim:

To draw the V-1 characteristics of Zener diode and hence to find Zener Breakdown voltage.
Apparatus & Components: Zener diode, Resistor (470Ω), RPS, DMM, milliammeter, spring board, connecting wires.

Theory: A heavily doped crystal diode which even conducts in reverse bias condition is Called Zener diode. By varying the doping level, It is possible to manufacture Zener diodes with the breakdown voltages from 2Vto 200V.

Procedure:

Forward bias characteristics:

1. Circuit is constructed as shown in the circuit diagram.

2. Vary the voltage VF in steps of 0.1V by varying RPS voltage.

3. Measure the current IF using milliammeter and tabulate the values.

4. Plot the graph by considering VF along X-axis and IF along Y-axis and determine the value of knee voltage (VK).

Reverse bias characteristics:

1. Circuit is constructed as shown in the circuit diagram.

2. Vary the voltage VR in steps of 1V by varying RPS voltage.

3. Measure the current IR using milliammeter and tabulate the values.

4. Plot the graph by considering VR along X-axis and IR along Y-axis and determine the value of Zener breakdown voltage (VZ).

Result:

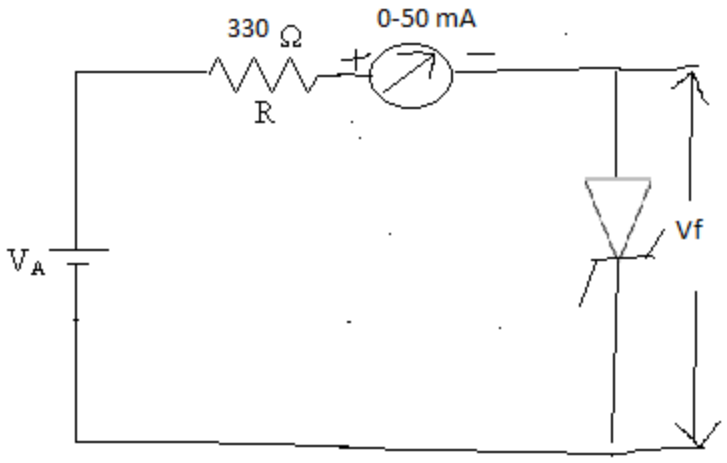
V-I characteristics of Zener diode is plotted and it is found that

1. Knee voltage (VK)=_____ V

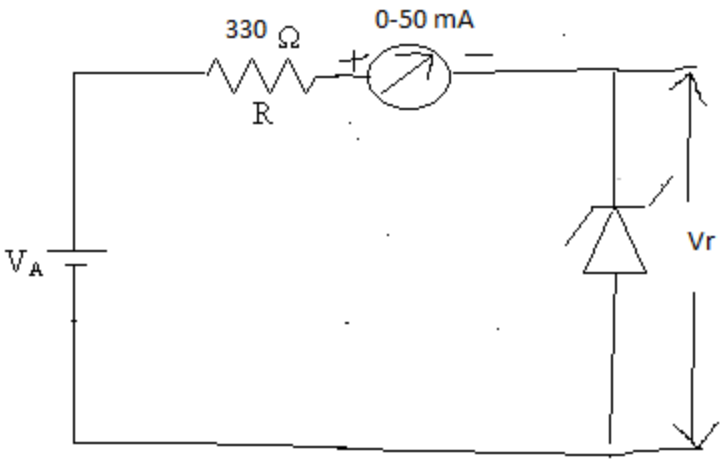
2. Zener breakdown voltage (VZ)=_____V

Circuit Diagram-:

Forward Characteristics-:



Reverse Characteristics-:



Tabular Column-:

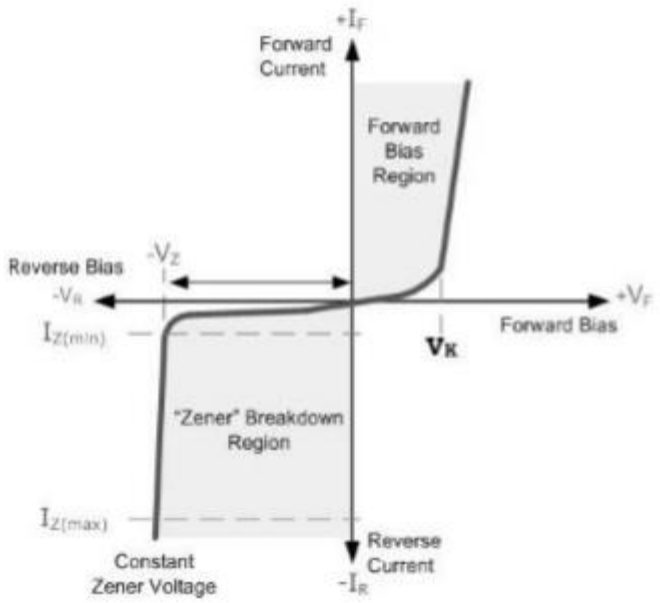
Forward Characteristics

Vi	Vf	If

Reverse Characteristics-:

Vi	Vr	Ir

Model Graph-:


+I_F
Forward Current
Forward Bias Region
Reverse Bias
-V_Z
-V_R
+V_F
Forward Bias
I_Z(min)
V_K
"Zener" Breakdown Region
I_Z(max)
Reverse Current
-I_R
Constant Zener Voltage

EXPERIMENT NO:4

HALF WAVE RECTIFIER - WITHOUT AND WITH SHUNT CAPACITOR FILTER

AIM: a) To construct a half wave rectifier without shunt capacitor filter and to determine its ripple factor for different load resistors R_L.

b) To construct a rectifier with shunt capacitor filter and to determine the ripple factor for different values of capacitances.

c) To determine load regulation for different values of load resistor R_L

COMPONENTS AND EQUIPMENT:

Step down transformer, semiconductor diode (IN4001), resistors –2.2kΩ, 10kΩ , capacitors – 10μF, 22μF, 100μF, resistance box.

PRINCIPLE:

The process of converting ac to pulsating DC voltage is called rectification.

The step down transformer is used to reduce ac voltage level to the permissible level for semiconductor device operations. During positive half cycle, the diode is forward biased, circuit current flows and half cycle of the input voltage appears across R_L. During the negative half cycle of the input, the diode is reverse biased and it does not conduct. Hence the output voltage is zero. Thus a pulsating DC output is obtained.

In case of Rectifier with Capacitor filter, the diode is ON during the positive half cycle which quickly charges the capacitor to peak voltage (Vm). The charging time is almost zero because there is no resistance in the charging path.

During the negative half cycle of the input, the capacitor tries to discharge through the diode. Since the diode is reverse biased, it tries to discharge through the load resistor. The discharging time constant is almost 100 times greater than that of charging time. Therefore even during the negative half cycle, the capacitor maintains sufficiently large voltage across R_L. The load sees a

nearly constant voltage across it. Increased value of the capacitor increases $V_{DC,}$ thereby reducing the magnitude of the ripple voltage.

PROCEDURE:

The circuit is connected as shown in the figure 1. The DC output voltage is measured across the load resistor, using a multimeter. Thus V_{DC} is obtained. The ac-ripple component present in the output is measured by blocking DC by using a 10μF capacitor. Ripple factor is a measure of purity of the DC and is calculated as the ratio of V_{ac} to V_{DC}.

The shunt capacitor filter is connected to the above circuit as shown in figure 2 with R_L=10KΩ. Ripple factor is calculated with the same procedure as above for four values of capacitances. It is seen that the ripple factor is very low since the shunt capacitor filters the ac component present at the output of the half wave rectifier.

RESULT:

a) A half wave rectifier without shunt capacitor filter has been constructed and its ripple factor determined for different values of R_L.

b) The shunt capacitor filter was connected to the rectifier and the ripple factor

has been calculated for different values of capacitances.

HALF WAVE RECTIFIER WITHOUT SHUNT CAPACITOR FILTER

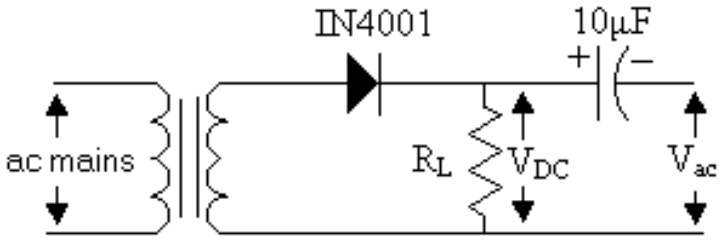


Fig 1.

TABULAR COLOUMN

R_L KΩ	V_{DC} (V)	V_{ac} (V)	Ripple factor $\gamma = V_{ac}/ V_{DC}$
2.2			
10			

HALF WAVE RECTIFIER WITH SHUNT CAPACITOR FILTER

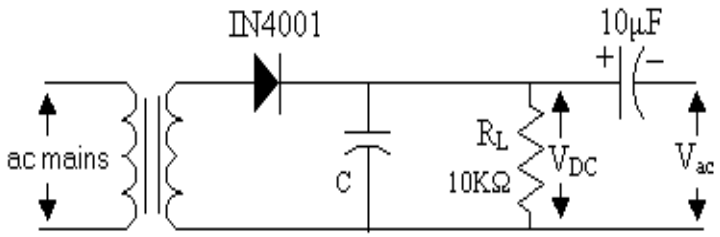


Fig 2.

TABULAR COLOUMN

C μf	V_{DC} (V)	V_{ac} (V)	Ripple factor $\gamma = Vac/ V_{DC}$
22			
100			

EXPERIMENT NO:5

BRIDGE RECTIFIER WITHOUT AND WITH SHUNT CAPACITOR FILTER

AIM: a) To construct a bridge (full wave) rectifier without shunt capacitor filter and to determine its ripple factor for different load resistors R_L.

b) To connect a shunt capacitor filter to the rectifier and to determine the ripple factor for different values of capacitances.

c) To determine load regulation for different values of load resistor R_L.

COMPONENTS AND EQUIPMENT: Step down transformer, diodes IN4001(4), resistance box, capacitors -10μF, 22 μF, 100 μF, resistors- 2.2KΩ, 10KΩ ,multimeter, patch cords and clips.

PRINCIPLE: The process of converting ac to pulsating DC is called rectification. A bridge rectifier is a full wave rectifier. Bridge rectifier uses four diodes in a bridge configuration and eliminates the need for a step down transformer with center tap.

During positive half cycle diode D_1 and D_3 are forward biased and diodes D_2 and D_4 are reverse biased. Current flows from A through D_1, R_L from (M to N) and D_3 to B.

During negative half cycle of input, diode D_2 and D_4 are forward biased and diodes D_1 and D_3 are reverse biased. Current flows from D through D_2, RL (from M to N) and D_3 to B).It is seen that current flows through R_L in the same direction during both the half cycles. The output is a pulsating dc.

Advantages: It uses smaller transformers and is suitable for high-voltage applications.

Also it has less PIV (Peak Inverse Voltage) rating per diode.

PROCEDURE: Circuit connections are made as shown in the figure 1. The output voltage V_{DC} is measured across R_L using a multimeter. The ac ripple component present in the output V_{ac} is measured by blocking dc using 10μF capacitor. Ripple factor is a measure of purity of dc and is calculated as a ratio of V_{ac} to V_{DC}. The above procedure is repeated for different values of R_L. The shunt capacitor filter is connected to the above circuit as shown in figure 2 with R_L=10KΩ. Ripple factor is calculated with the same procedure as above for four values of capacitances. It is seen that the ripple factor is very low since the shunt capacitor filters the ac component present at the output of the half wave rectifier.

RESULT: Bridge Rectifier without shunt capacitor filter has been constructed and studied. The ripple factor has been determined for different values of load resistor (R_L).

Bridge rectifier with shunt capacitor filter has been constructed and studied and the ripple factor determined for different values of capacitor.

Bridge rectifier without shunt capacitor filter

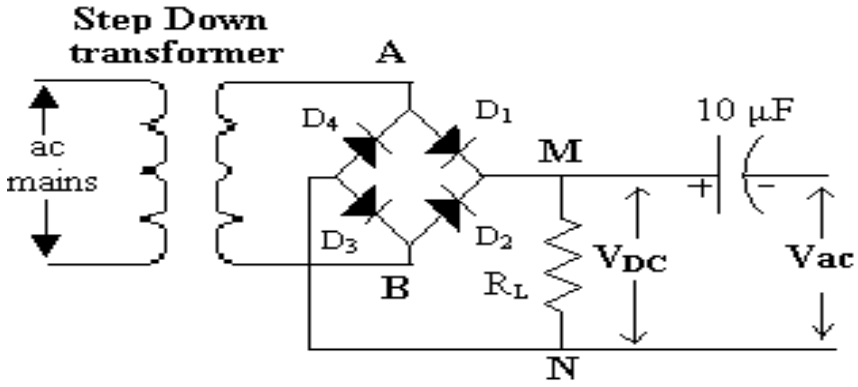


Fig 1

TABULAR COLUMN

R_L KΩ	V_{DC} (V)	V_{ac} (V)	Ripple factor $\gamma = V_{ac} / V_{DC}$
2.2			
10			

BRIDGE RECTIFIER WITH SHUNT CAPACITOR FILTER

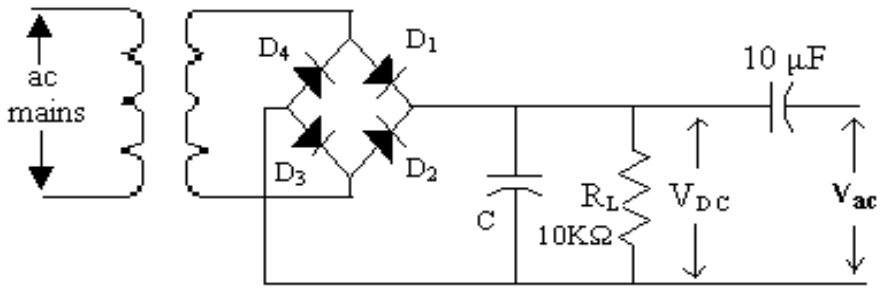


Fig 2

TABULAR COLUMN

C μF	V_{DC} (V)	V_{ac} (V)	Ripple factor $\gamma = V_{ac}/ V_{DC}$
22			
100			

EXPERIMENT NO:6

Study of Clipping and Clamping Circuits

AIM

To realize different clipping, clamping circuits and Voltage Multiplier circuits and observe the waveforms.

COMPONENTS REQUIRED-:

Step down transformer with varying secondary voltages, diodes IN4001- 4, electrolytic capacitors -10 μF (4) ,100k, 1k CRO and multimeter.

THEORY -:

Clipping Circuits -:Clipping circuits are nonlinear wave shaping circuits. A clipping circuit is useful to cut off the positive or negative portions of an input waveform. Clipping circuits are also known as voltage limiters or slicers.

Positive clipper -:The positive half cycle is clipped by diode and only the drop across diode will appear across the load. During negative half cycle, the diode does not conduct. Since RL >> R, the output voltage will be close to input voltage during negative half cycle.

Negative clipper-: The negative half cycle is clipped by diode and only the drop across diode will appear across the load. During positive half cycle, the diode does not conduct .Since RL >> R, the output voltage will be close to input voltage during the positive half cycle.

Clamping Circuit –:Clamping is a function which must be frequently performed with a periodic waveform in the establishment of the recurrent positive or negative extremity at some constant reference level. Clamping circuits are also referred to as dc restorer or dc inserter. A positive clamper adds positive dc level and a negative clamper adds a negative dc level. A positive clamper clamps a negative extremity of the input signal to the reference voltage level. A negative clamper adds to negative dc level by clamping the positive extremity of the input to the reference voltage level.

Voltage Multiplier-; A voltage multiplier is a circuit which produces a greater DC output voltage than ac input voltage to the rectifiers.

A voltage doubler uses two stages of R and C to approximately double the DC voltage that would have been obtained from a single-stage rectifier. A voltage tripler is a three-stage voltage multiplier. Multipliers are used in many applications where high voltages with low currents are required such as for accelerating purposes in a Cathode ray Tube.

PROCEDURE

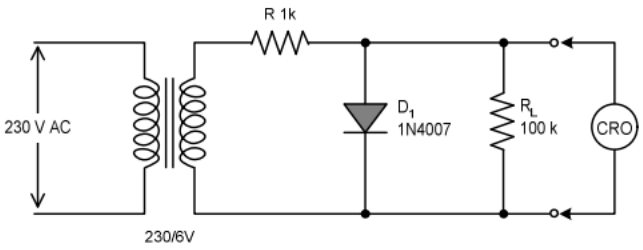
The circuits are wired as in the circuit diagram. Connect the input terminals to 230V ac supply and the output terminals to a CRO for observing the output waveforms.

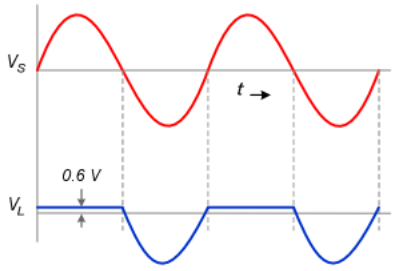
RESULT:

Clipping and Clamping Circuits are constructed and the output waveforms are observed on CRO Voltage multiplier has been constructed and the peak input voltage, double output, triple output and quadruple output has been calculated and compared.

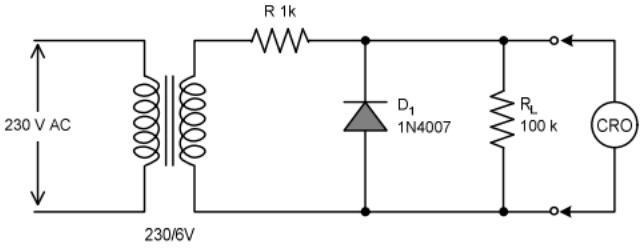
Circuit Diagram-:

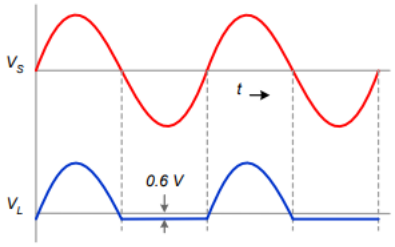
Positive clipper



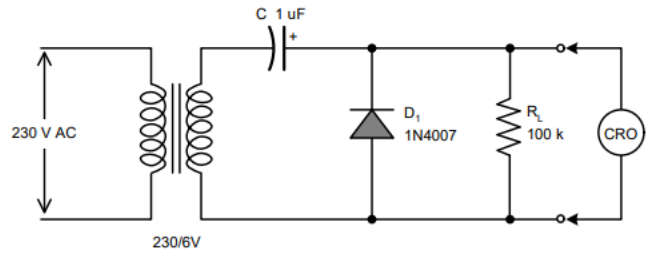


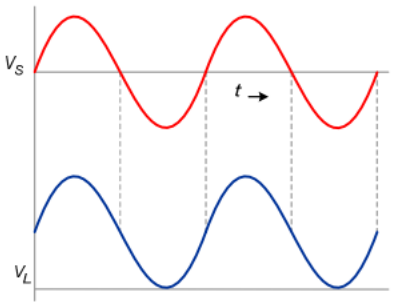
Negative clipper



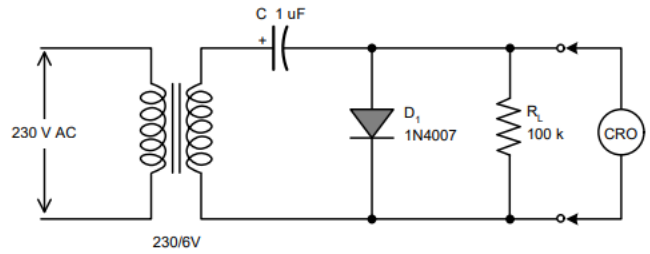


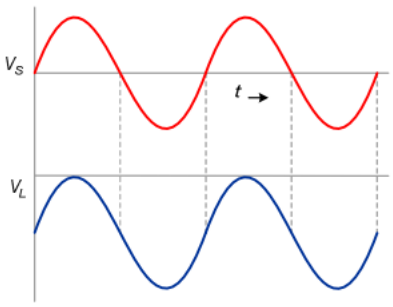
Positive clamping Circuit





Negative clamping Circuit





EXPERIMENT NO – 7

Study of single stage CE amplifier (frequency response, input and output impedances in mid-band)

Aim: Study of single stage CE amplifier and its frequency response, input and output impedances in mid-band

Equipment's: Transistor, resistors, capacitors, signal generator, DC power supply, CRO, DRB

Principle:

It is the most widely used amplifier. It provides MODERATE input and output impedance, high voltage and current gain. It introduces 180 degree of phase inversion between input and output signals. When the input signal is coupled to base-emitter junction of the transistor, the largely varying collector current flows through the collector which produces the amplified output voltage.

Input impedance

The input impedance of an amplifier can be tens of ohms, (Ohms Ω) to a few thousand ohms, (kilo-ohms kΩ) for bipolar based transistor circuits. The input impedance may depend upon the source supply feeding the amplifier

Output impedance

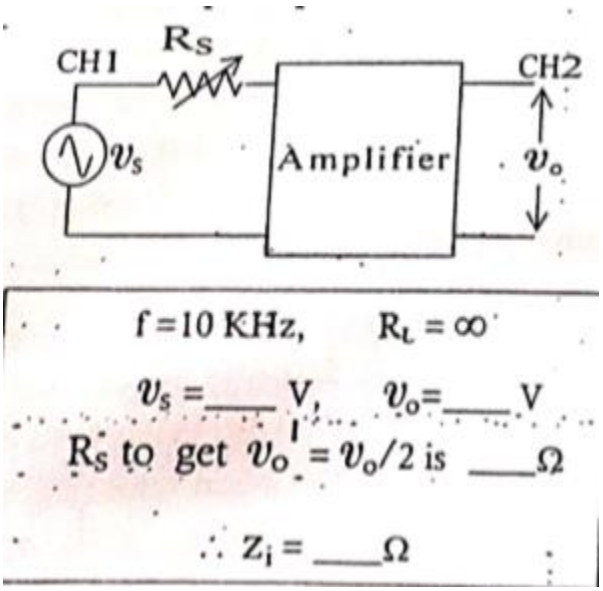
the output impedance may also vary according to the load impedance, RL across the output terminals.

Procedure

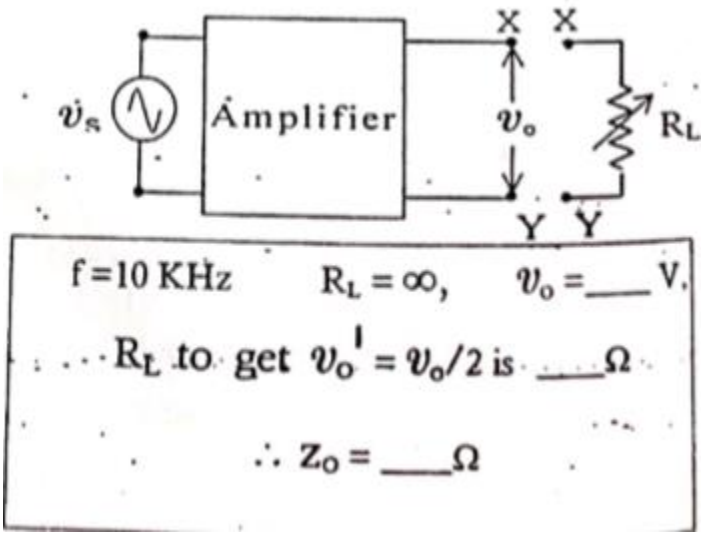
1.Components are checked for their correctness.
2. Connections are made as shown in figure.
3. Input signal is adjusted to 50mV.
4. Frequency of the input signal is varied in steps, as given in the tabular column and corresponding output voltage is measured on CRO and values are tabulated.
5. Frequency response curve is plotted on semi log graph sheet and bandwidth is calculated

6. To measure input impedance we can use DRB at the input stage and remove load resistance RL, DRB adjusted until output voltage equal to half of the previous output voltage

Input impedance



Input impedance



7. To measure output impedance we can use DRB at the output stage and remove input resistance Rs, DRB adjusted until output voltage equal to half of the previous output voltage.

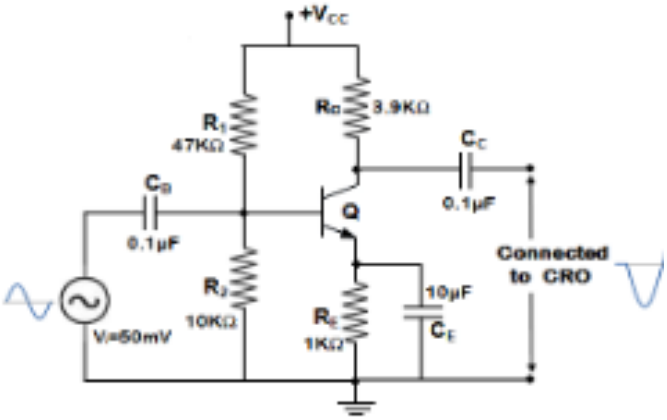
Result: CE amplifier circuit is constructed and its frequency response curve is studied. Bandwidth of the above constructed CE amplifier is equal to = ----------KHz

TABULAR COLOUM:

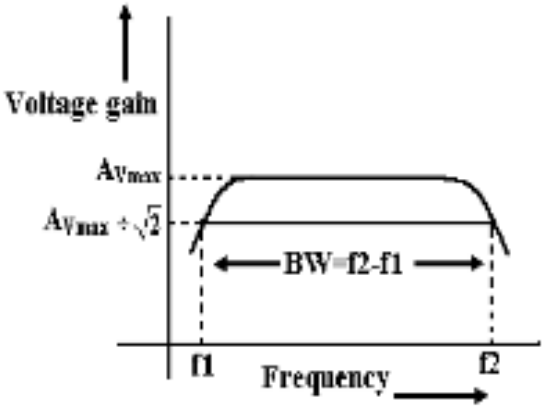
V_{in}=50mV

Frequency (Hz)	Output Voltage (volts)	Gain $Av=\frac{Vo}{Vi}$
100		
200		
300		
500		
1K		
2K		
3K		
5K		
7K		
10K		
20K		
30K		
50K		
70K		
100K		
200K		
300K		
400K		
500K		
700K		
1M		
2M		

CIRCUIT DIAGRAM:



SPECIMEN GRAPH:



EXPERIMENT NO - 8

Verification of truth tables for AND, OR, NOT, NAND, NOR and Exclusive OR (EX-OR) Gates using respective ICs. Realization of XOR and XNOR by using basic gates

Aim: Verification of truth tables for AND, OR, NOT, NAND, NOR and Exclusive OR (EX-OR) Gates. Realization of XOR and XNOR using basic gates.

Equipment's: Digital trainer kit, ICs – 7400, 7408, 7402, 7432, 7404, 7486, Patch chords.

Principle: Logic gates are electronic circuits which perform logical functions on one or more inputs to produce one output. The function of each gate is defined by a truth table, which specifies the output state for each possible combination of input states. In digital logic only two voltage levels or states are allowed and these states are generally referred to as Logic "1" or Logic "0", High or Low.

a) **Verification of truth tables for AND, OR, NOT, NAND, NOR and Exclusive gates.**

NOT Gate: It is the simplest possible gate and is called an "inverter," or a NOT gate. It takes one bit as input and produces an inverted or reversed output. The logic table for NOT gate and its symbol are shown below.

AND Gate: It performs logical multiplication based on the combinations of its inputs. AND gate produces an output as 1, when all its inputs are 1; otherwise the output is 0. This gate can have minimum 2 inputs but output is always one. Its output is 0 when any input is 0.

OR Gate: It performs logical addition based on the combinations of its inputs. OR gate produces an output as 1, when any or all its inputs are 1; otherwise the output is 0. This gate can have minimum 2 inputs but output is always one. Its output is 0 when all input is 0.

NAND Gate: NAND gate is actually a series of AND gate with NOT gate. If we connect the output of an AND gate to the input of a NOT gate, this combination will work as NOT-AND or NAND gate. Its output is 1 when any or all inputs are 0, otherwise output is 1.

NOR Gate: NOR gate is a series of OR gate with NOT gate. If we connect the output of an OR gate to the input of a NOT gate, this combination will work as NOT-OR or NOR gate. Its output is 0 when any or all inputs are 1, otherwise output is 1.

XOR Gate: X-OR gate has two inputs and one output. It produces an output as 1, when number of 1's at its inputs is **odd**, otherwise output is 0.

XNOR Gate: XNOR gate has two inputs and one output. It produces an output as 1, when both the inputs are high, otherwise output is 0.

(b) Realization of XOR and XNOR using basic gates:

Realization of XOR and XNOR using basic gates. With the help of IC 7432, 7404 and 7408 verifying the XOR and XNOR truth table.

Procedure:
1. Check the Patch chords for proper working.
2. Connect the trainer kit to ac power supply.
3. Place the Respective IC in the IC Tray and connect the VCC and Gnd.
4. Apply various input combinations and observe output for each one.
5. Verify the truth table for each input/ output combination.
6. Repeat the process for all other logic gates.
7. Switch off the ac power supply.

Result: The logic gates for AND, OR, NOT, NAND, NOR and XOR gates was seen and the truth table verified. Realization of XOR and XNOR using basic gates verified with the corresponding truth table

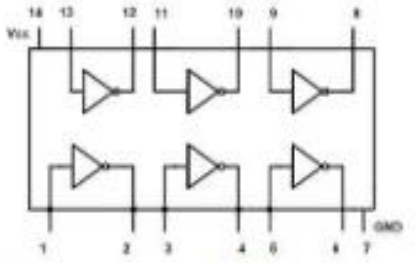
NOT Gate:

$Y = \overline{A}$

Symbol

Input	Output
A	Y
0	1
1	0

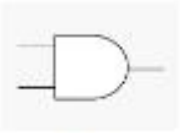
Truth table



Pin Diagram: IC 7404

AND Gate:

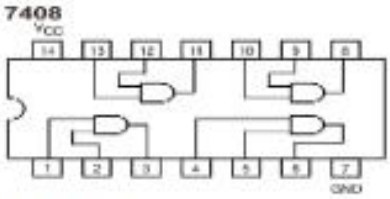
AND $Y = AB$



Symbol

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table



Pin Diagram:

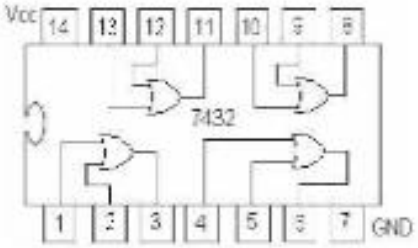
OR Gate:

OR $Y = A+B$

Symbol

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

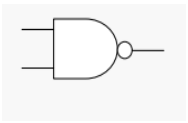
Truth table



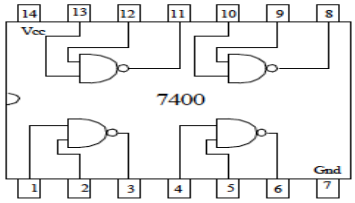
Pin Diagram:

NAND Gate:

NAND $Y = \overline{AB}$



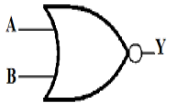
A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0



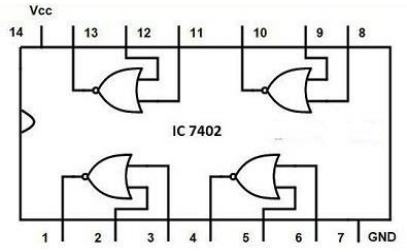
Symbol Truth Table Pin diagram:

NOR Gate:

NOR $Y = \overline{A+B}$



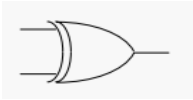
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0



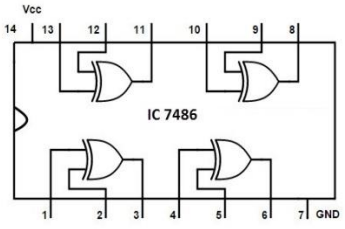
Symbol Truth Table Pin Diagram

XOR Gate:

XOR $Y = A \oplus B$

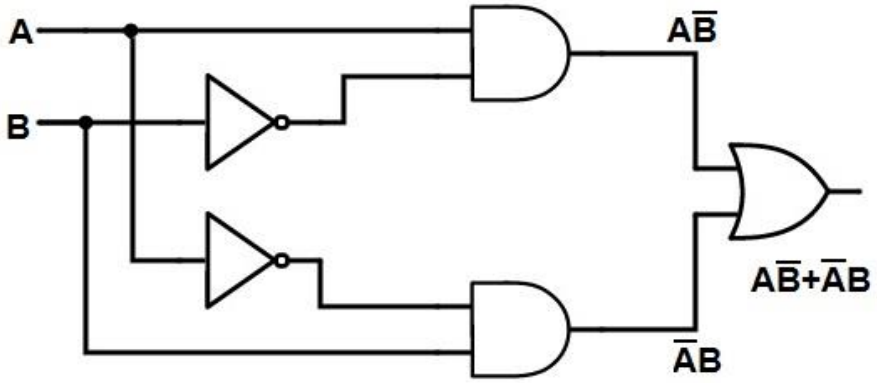


A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0



Symbol Truth Table Pin Diagram

(b) Realization of XOR and XNOR using basic gates.

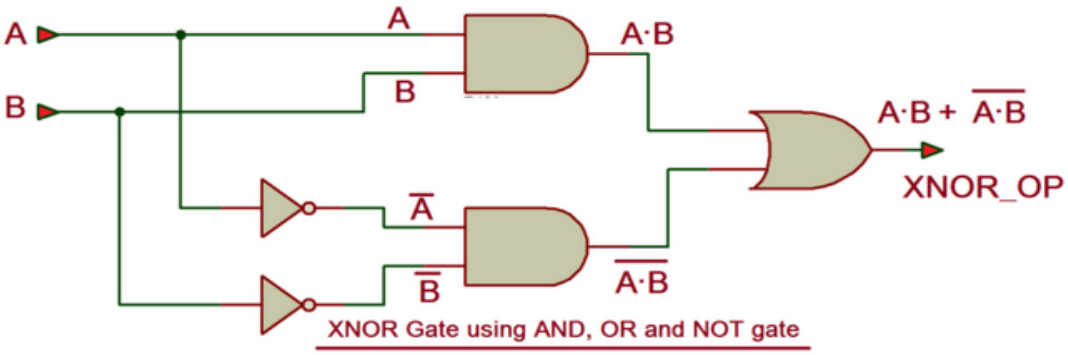


A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

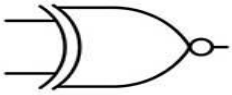
XOR $Y = A \oplus B$

Symbol

Truth Table



XNOR



A	B	Output
0	0	1
1	0	0
0	1	0
1	1	1

EXPERIMENT NO - 9

Realization of AND, OR, NOT using Universal Gates, NAND and NOR.

Aim: Realization of Basic Gates with the help of universal gates.

Equipment's: Digital trainer kit, ICs – 7400 and 7402, Patch chords.

Principle: By using only NAND gates and NOR gates, we can realize all logic functions: AND, OR, NOT, X-OR, and NOR. So this gate is also called a universal gate.

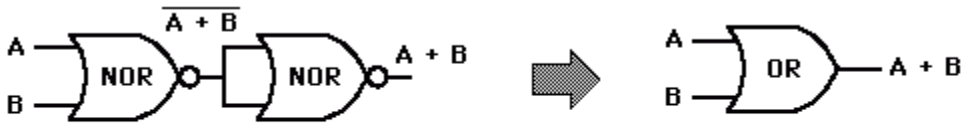
Procedure:
1. Check the Patch chords for proper working.
2. Connect the trainer kit to ac power supply.
3. Place the Respective IC in the IC Tray and connect the VCC and Gnd.
4. Apply various input combinations and observe output for each one.
5. Verify the truth table for each input/ output combination.
6. Repeat the process for all other logic gates.
7. Switch off the ac power supply.

Result: AND, OR and NOT gates using NAND and NOR was constructed and the truth table verified.

NOR as NOT Gate:

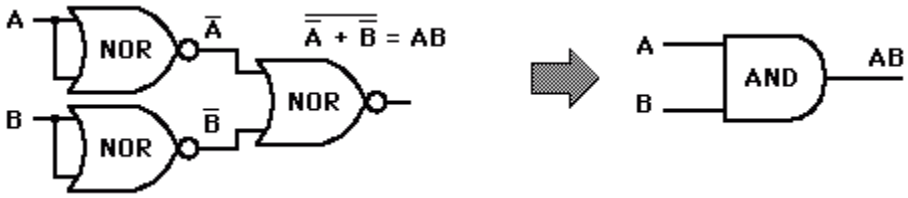
NAND Equivalent Symbol

NOR as OR Gate:



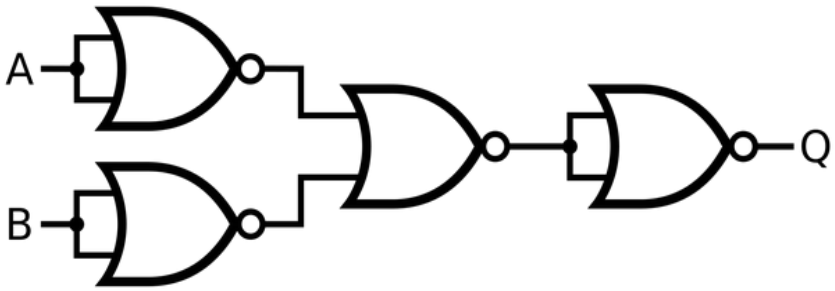
NAND Equivalent Symbol

NOR as AND Gate:

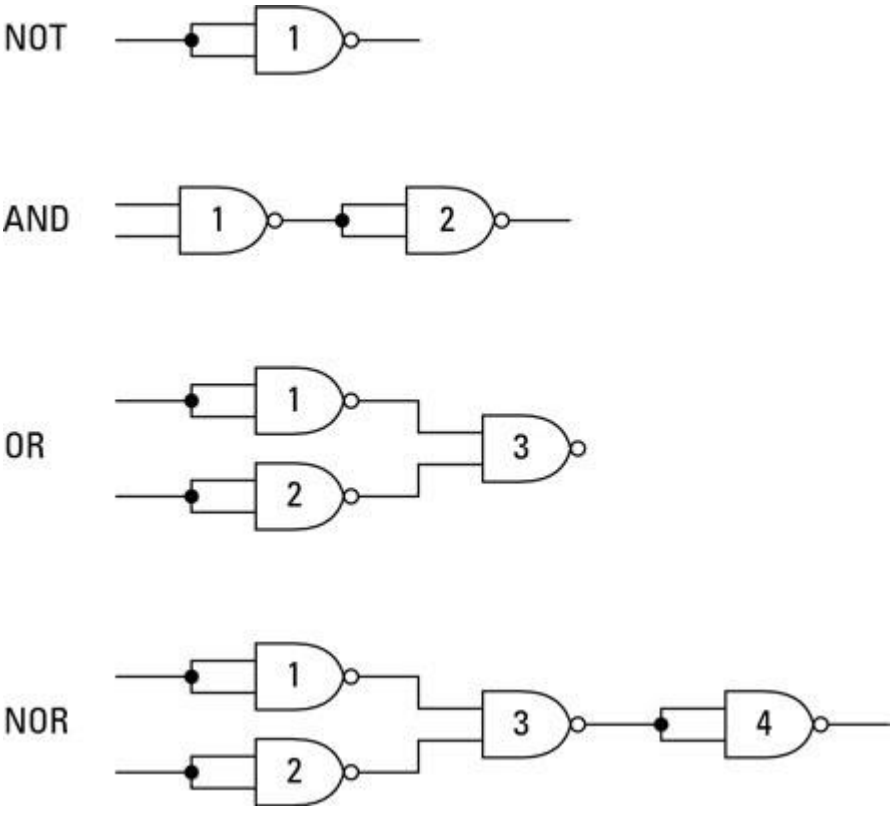


NAND Equivalent Symbol

NOR as NAND Gate:



Realization of NOT, AND , OR and NOR gate using NAND



EXPERIMENT NO – 10

Binary to Gray and Gray to Binary code conversion and parity checker using XOR gates IC 7486.

Aim: Realization of Binary to Gray and Gray to Binary code conversion and parity checker using XOR gates IC 7486.

Equipment's: Digital trainer kit, IC 7486, Patch chords.

Principle: By using IC 7486 we can construct Binary to Gray and Gray to Binary code conversion.

4-bit Binary to Gray code converter:

The input to the 4-bit binary-to-Gray code converter circuit is a 4-bit binary and the output is a 4- bit Gray code. There are 16 possible combinations of 4-bit binary input and all of them are valid. Hence no don't cares. The 4-bit binary and the corresponding Gray code are shown in the conversion table. From the conversion table, we observe that the expression for the outputs G3, G2, G1 and G0 are as follows:

$G3=B3$
$G2=G2 \oplus G3$
$G1=G1 \oplus G2$
$G0=G0 \oplus G1$

Gray to binary conversion

the Most Significant Bit (MSB) of the binary code is always equal to the MSB of the given binary number. Other bits of the output binary code can be obtained by checking gray code bit at that index. If current gray code bit is 0, then copy previous binary code bit, else copy invert of previous binary code bit. There are four inputs and four outputs. The input variable is defined as G3, G2, G1, G0 and the output variables are defined as B3, B2, B1, B0. From the truth table, combinational circuit is designed. The logical expressions are defined as:

$B3=G3$

B2=G2⊕G3
B1= G1⊕G2⊕G3
B0= G0⊕ G1⊕G2⊕G3

Even Parity Generator:

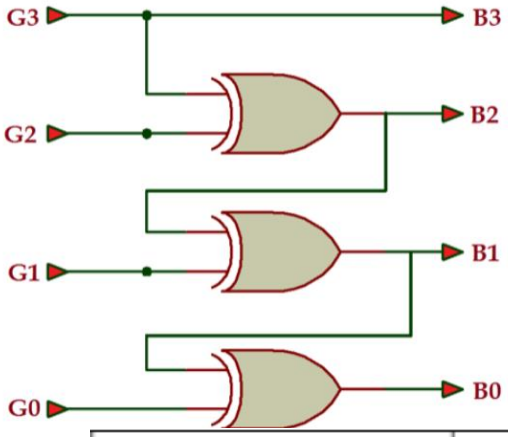
In even parity bit scheme, the parity bit is '0' if there are even number of 1s in the data stream and the parity bit is '1' if there are odd number of 1s in the data stream. In a 3-bit message is to be transmitted with an even parity bit. Let the three inputs A, B and C are applied to the circuit and output bit is the parity bit P. The total number of 1s must be even, to generate the even parity bit P.

P=A⊕B⊕C

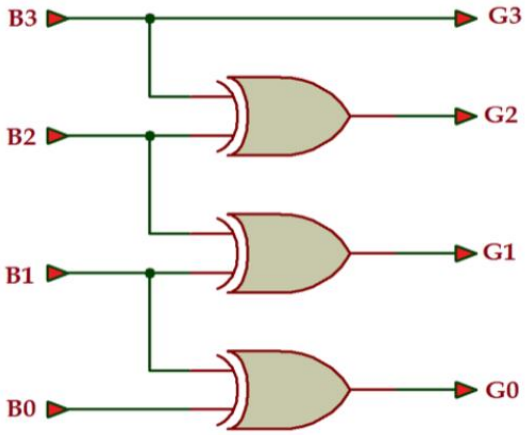
Procedure:
1. Check the Patch chords for proper working.
2. Connect the trainer kit to ac power supply.
3. Place the Respective IC in the IC Tray and connect the VCC and Gnd.
4. Apply various input combinations and observe output for each one.
5. Verify the truth table for each input/ output combination.
6. Repeat the process for all other logic gates.
7. Switch off the ac power supply.

Result: By using IC 7486 Binary to Gray and Gray to Binary code conversion was constructed and the truth table verified. Even parity checker also verified with the truth table.

4-bit Gray to binary code converter

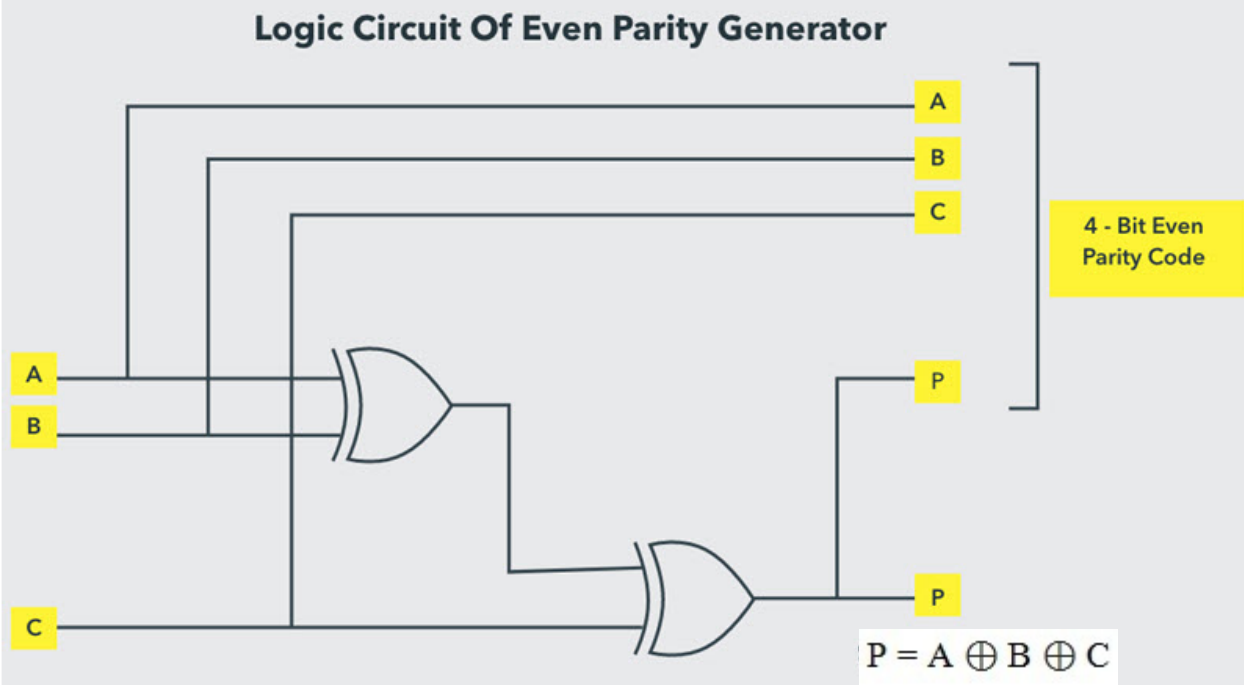


4-bit Binary to Gray code converter



Inputs				Outputs			
B3	B2	B1	B0	G3 (V)	G2 (V)	G1 (V)	G0 (V)
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

parity checker using XOR gates IC 7486.



3-bit message			Even parity bit generator (P)	
A	B	C	Y	
0	0	0	0	
0	0	1	1	
0	1	0	1	
0	1	1	0	
1	0	0	1	
1	0	1	0	
1	1	0	0	
1	1	1	1	

EXPERIMENT NO – 11

2-bit comparator using logic gates

Aim: Constructing 2-bit comparator using logic gates and verifying the truth table.

Equipment's: Digital trainer kit, IC's, Patch chords.

Principle: By using IC's we can Constructing 2-bit comparator using logic gates and verifying the truth table.

Comparator: A digital comparator or magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number.

2-bit magnitude comparator:

A comparator used to compare two binary numbers each of two bits is called a 2-bit magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to and greater than between two binary numbers.

Procedure:

1. Check the Patch chords for proper working.
2. Connect the trainer kit to ac power supply.
3. Place the Respective IC in the IC Tray and connect the VCC and Gnd.
4. Apply various input combinations and observe output for each one.
5. Verify the truth table for each input/ output combination.
6. Repeat the process for all other logic gates.
7. Switch off the ac power supply.

The truth table for a 2-bit comparator is given below:

INPUT				OUTPUT		
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Result: By using logic gates 2-bit comparator constructed and verifying the truth table.

EXPERIMENT NO – 12

Multiplexer and De-multiplexer

Aim: Constructing 4x1 Multiplexer and 4x1 De-multiplexer using logic gates and verifying the truth table.

Equipment's: Digital trainer kit, IC's, Patch chords.

1) Multiplexer

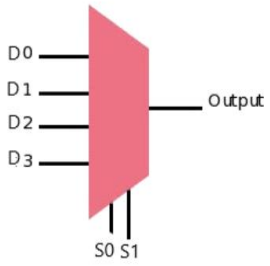
Multiplexer is a device that has multiple inputs and a single line output. The select lines determine which input is connected to the output, and also to increase the amount of data that can be sent over a network within certain time. It is also called a data selector.

Multiplexers are classified into four types:

a) 2-1 multiplexer (1 select line)
b) 4-1 multiplexer (2 select lines)
c) 8-1 multiplexer(3 select lines)
d) 16-1 multiplexer (4 select lines)

1.1) 4x1 Multiplexer

4x1 Multiplexer has four data inputs D0, D1, D2 & D3, two selection lines S0 & S1 and one output Y. The block diagram of 4x1 Multiplexer is shown in the following figure.One of these 4 inputs will be connected to the output based on the combination of inputs present at these two selection lines. 4x1 Multiplexer is shown below



2) De-multiplexer

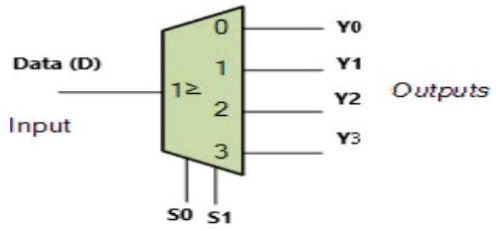
De-multiplexer is also a device with one input and multiple output lines. It is used to send a signal to one of the many devices. The main difference between a multiplexer and a de-multiplexer is that a multiplexer takes two or more signals and encodes them on a wire, whereas a de-multiplexer does reverse to what the multiplexer does.

De-multiplexer are classified into four types:

a)1-2 demultiplexer (1 select line)
b)1-4 demultiplexer (2 select lines)
c)1-8 demultiplexer (3 select lines)
d)1-16 demultiplexer (4 select lines)

2.2) 1x4 De-multiplexer

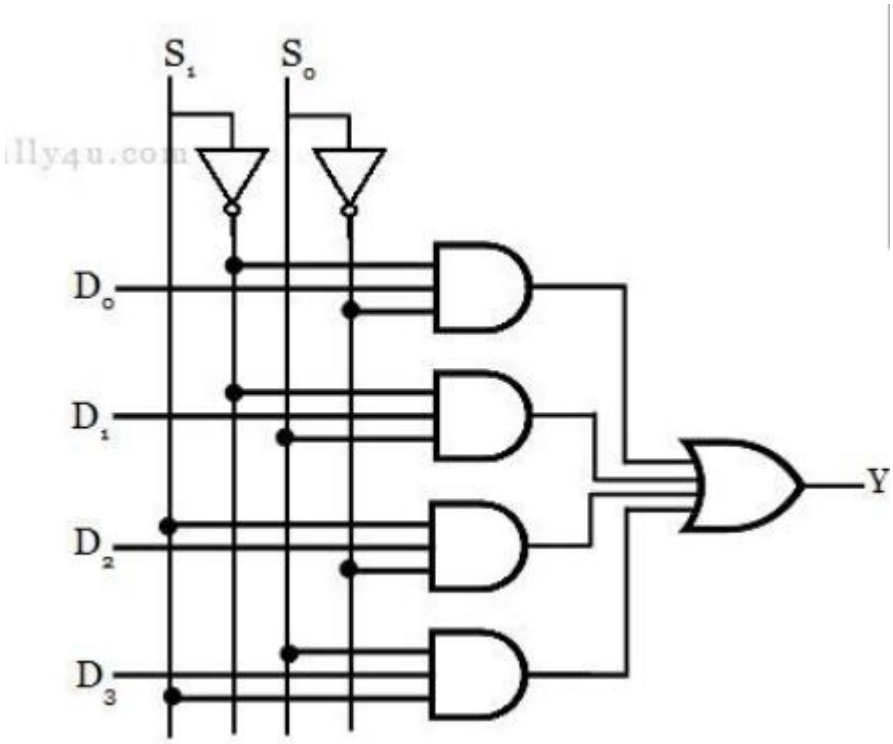
1x4 De-Multiplexer has one input Data(D), two selection lines, S0 & S1 and four outputs Y0, Y1, Y2 & Y3. The block diagram of 1x4 De-Multiplexer is shown in the following figure.



Procedure:
1. Check the Patch chords for proper working.
2. Connect the trainer kit to ac power supply.
3. Place the Respective IC in the IC Tray and connect the VCC and Gnd.
4. Apply various input combinations and observe output for each one.
5. Verify the truth table for each input/ output combination.
6. Repeat the process for all other logic gates.
7. Switch off the ac power supply.

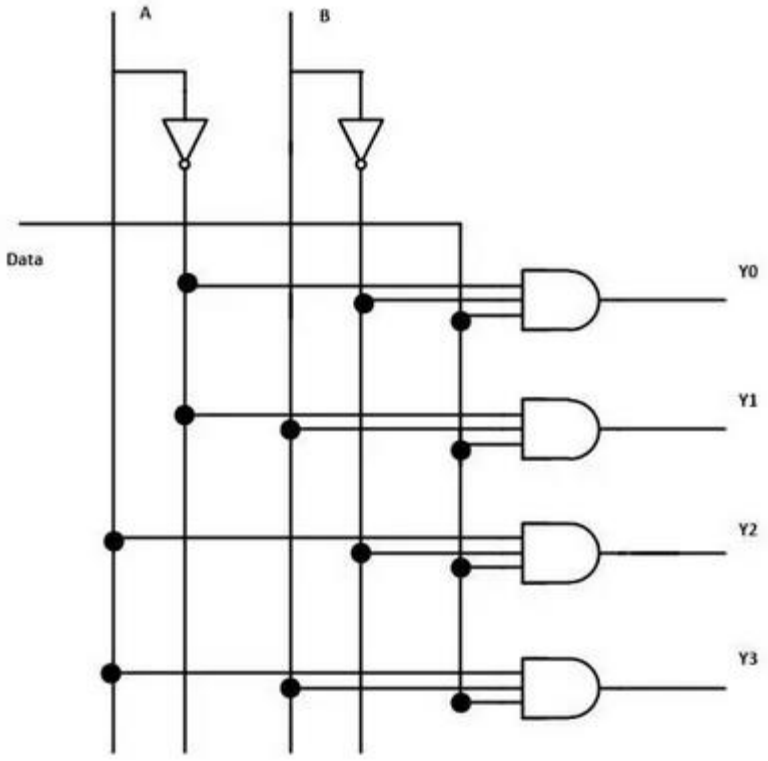
Selection Lines		Output
S0	S1	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Figure-3:Truth table of 4x1 Multiplexer



Selection Inputs		Outputs			
S0	S1	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	D
0	1	0	0	D	0
1	0	0	D	0	0
1	1	D	0	0	0

Figure-5:Truth table of 1x4 De-Multiplexer



Result: 4x1 Multiplexer and 4x1 De-multiplexer constructed using logic gates and verifying the truth table.